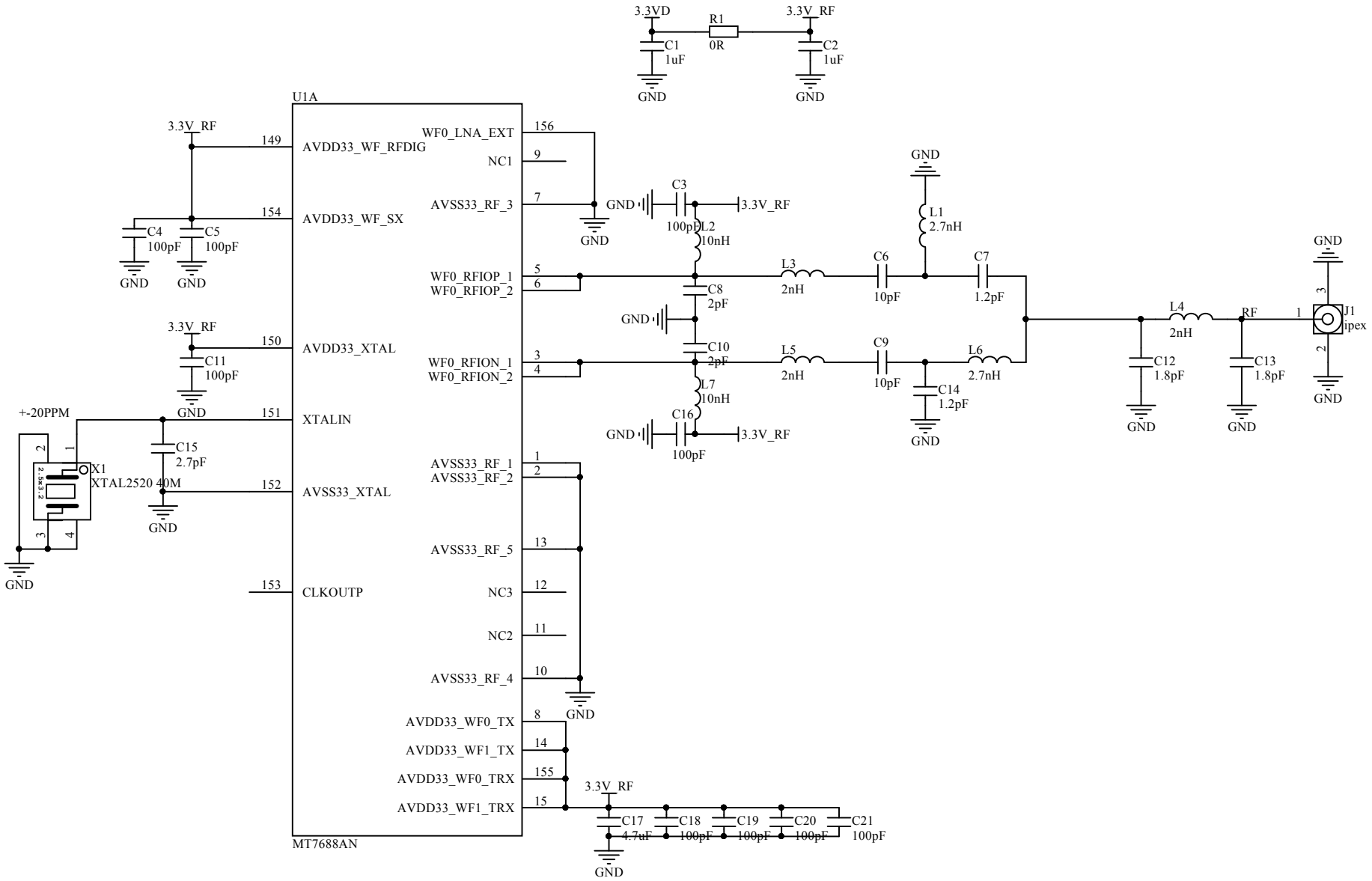
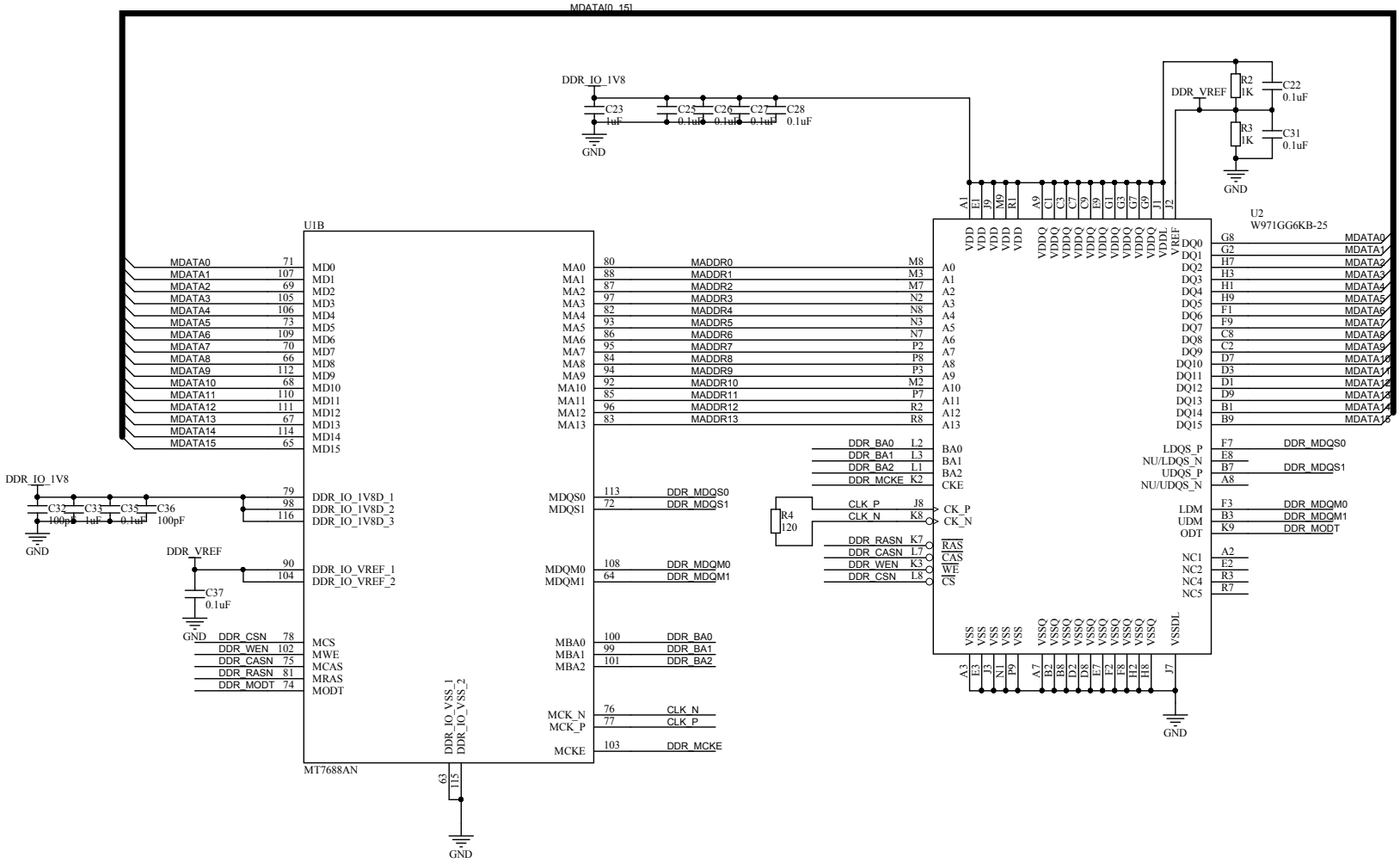
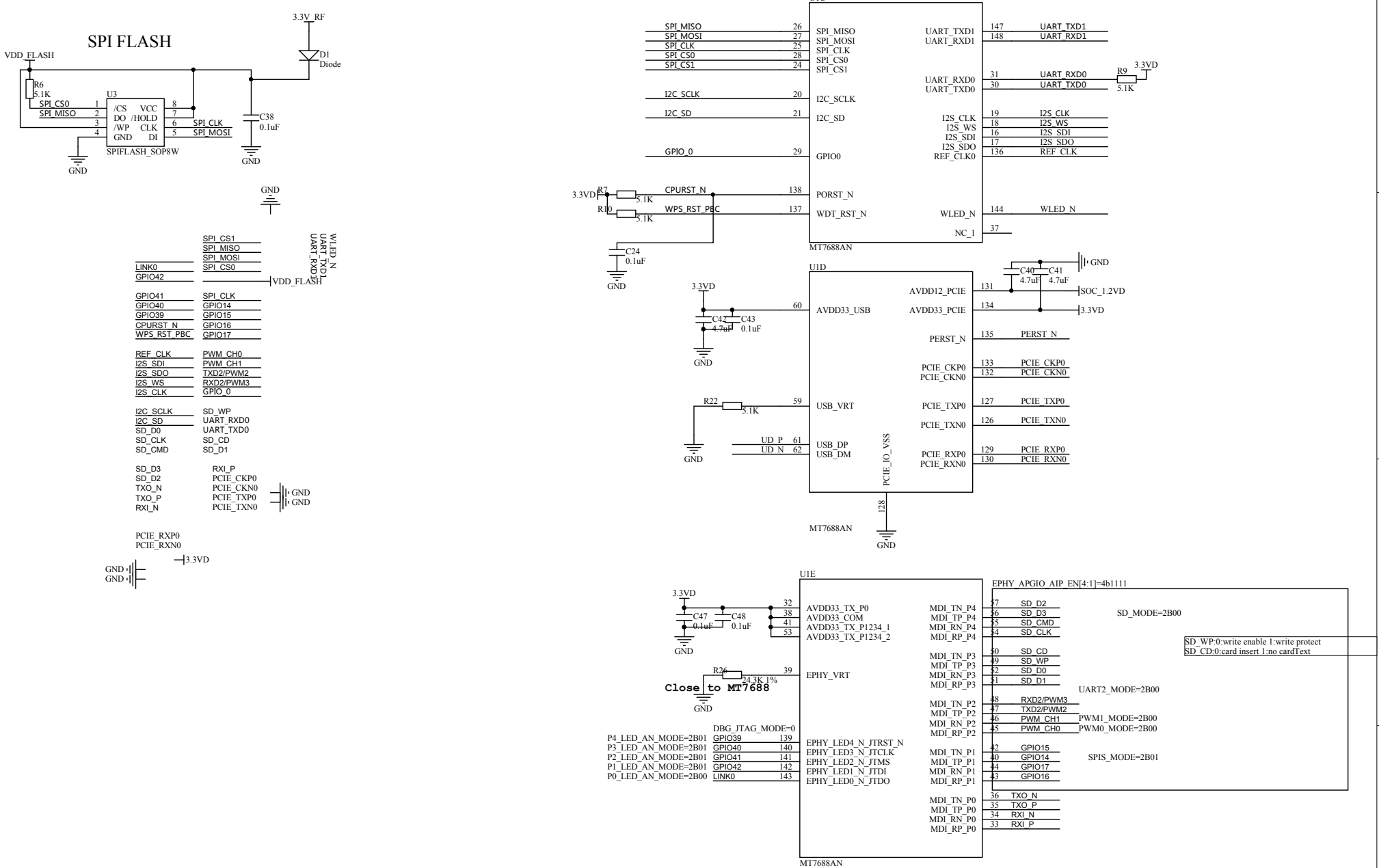
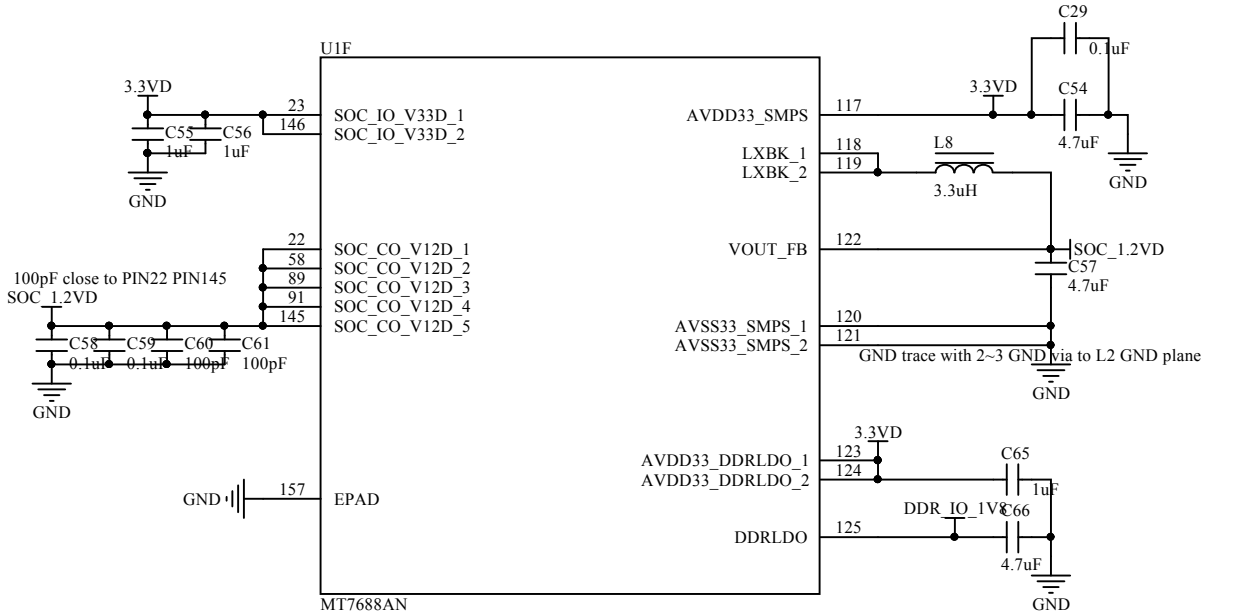
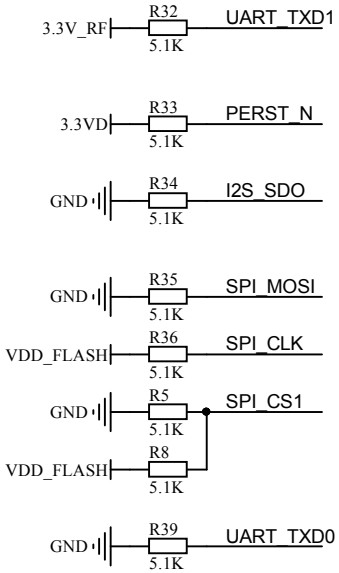

3.3VD
R1
0R
3.3V_RF
C1
1uF
C2
1uF
GND
GND
U1A
3.3V_RF
149
AVDD33_WF_RFDIG
154
AVDD33_WF_SX
C4
100pF
C5
100pF
GND
GND
3.3V_RF
150
AVDD33_XTAL
C11
100pF
GND
+-20PPM
GND
151
XTALIN
C15
2.7pF
X1
XTAL2520 40M
152
AVSS33_XTAL
GND
GND
153
CLKOUTP
WF0_LNA_EXT
156
NC1
9
AVSS33_RF_3
7
GND
C3
100pF
3.3V_RF
L2
10nH
GND
L1
2.7nH
WF0_RFIOP_1
5
WF0_RFIOP_2
6
L3
2nH
C6
10pF
C7
1.2pF
C8
2pF
GND
GND
L4
2nH
RF
1
J1
ipex
3
2
GND
GND
C10
2pF
WF0_RFION_1
3
WF0_RFION_2
4
L5
2nH
C9
10pF
L6
2.7nH
L7
10nH
C12
1.8pF
C13
1.8pF
C14
1.2pF
GND
GND
GND
C16
100pF
GND
3.3V_RF
AVSS33_RF_1
1
AVSS33_RF_2
2
AVSS33_RF_5
13
NC3
12
NC2
11
AVSS33_RF_4
10
GND
AVDD33_WF0_TX
8
AVDD33_WF1_TX
14
AVDD33_WF0_TRX
155
AVDD33_WF1_TRX
15
3.3V_RF
C17
4.7uF
C18
100pF
C19
100pF
C20
100pF
C21
100pF
GND
MT7688AN


MDATA[0..15]
U1B
MT7688AN
MDATA0 71
MDATA1 107
MDATA2 69
MDATA3 105
MDATA4 106
MDATA5 73
MDATA6 109
MDATA7 70
MDATA8 66
MDATA9 112
MDATA10 68
MDATA11 110
MDATA12 111
MDATA13 67
MDATA14 114
MDATA15 65
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
DDR_IO_1V8
C23 1uF
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
GND
DDR_IO_1V8
C32 100pF
C33 1uF
C35 0.1uF
C36 100pF
GND
79
98
116
DDR_IO_1V8D_1
DDR_IO_1V8D_2
DDR_IO_1V8D_3
DDR_VREF
C37 0.1uF
GND
90
104
DDR_IO_VREF_1
DDR_IO_VREF_2
DDR_CSN 78
DDR_WEN 102
DDR_CASN 75
DDR_RASN 81
DDR_MODT 74
MCS
MWE
MCAS
MRAS
MODT
DDR_IO_VSS_1
DDR_IO_VSS_2
63
115
GND
MA0 80 MADDR0
MA1 88 MADDR1
MA2 87 MADDR2
MA3 97 MADDR3
MA4 82 MADDR4
MA5 93 MADDR5
MA6 86 MADDR6
MA7 95 MADDR7
MA8 84 MADDR8
MA9 94 MADDR9
MA10 92 MADDR10
MA11 85 MADDR11
MA12 96 MADDR12
MA13 83 MADDR13
MDQS0 113 DDR_MDQS0
MDQS1 72 DDR_MDQS1
MDQM0 108 DDR_MDQM0
MDQM1 64 DDR_MDQM1
MBA0 100 DDR_BA0
MBA1 99 DDR_BA1
MBA2 101 DDR_BA2
MCK_N 76 CLK_N
MCK_P 77 CLK_P
MCKE 103 DDR_MCKE
DDR_IO_1V8
C22 0.1uF
R2 1K
DDR_VREF
R3 1K
C31 0.1uF
GND
U2
W971GG6KB-25
VDD A1 E1 J9 M9 R1
VDDQ A9 C1 C3 C7 C9 E9 G1 G3 G7 G9 J1 J2
VDDL
VREF
VSS A3 E3 J3 N1 P9
VSSQ A7 B2 B8 D2 D8 E7 F2 F8 H2 H8
VSSDL J7
GND
DDR_BA0 L2
DDR_BA1 L3
DDR_BA2 L1
DDR_MCKE K2
CLK_P J8
CLK_N K8
R4 120
DDR_RASN K7
DDR_CASN L7
DDR_WEN K3
DDR_CSN L8
BA0
BA1
BA2
CKE
CK_P
CK_N
RAS
CAS
WE
CS
DQ0 G8 MDATA0
DQ1 G2 MDATA1
DQ2 H7 MDATA2
DQ3 H3 MDATA3
DQ4 H1 MDATA4
DQ5 H9 MDATA5
DQ6 F1 MDATA6
DQ7 F9 MDATA7
DQ8 C8 MDATA8
DQ9 C2 MDATA9
DQ10 D7 MDATA10
DQ11 D3 MDATA11
DQ12 D1 MDATA12
DQ13 D9 MDATA13
DQ14 B1 MDATA14
DQ15 B9 MDATA15
LDQS_P F7 DDR_MDQS0
NU/LDQS_N E8
UDQS_P B7 DDR_MDQS1
NU/UDQS_N A8
LDM F3 DDR_MDQM0
UDM B3 DDR_MDQM1
ODT K9 DDR_MODT
NC1 A2
NC2 E2
NC4 R3
NC5 R7


SPI FLASH
3.3V_RF
D1
Diode
VDD_FLASH
R6
5.1K
SPI_CS0
SPI_MISO
U3
/CS VCC
DO /HOLD
/WP CLK
GND DI
SPI_CLK
SPI_MOSI
SPIFLASH_SOP8W
C38
0.1uF
GND
U1C
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS0
SPI_CS1
I2C_SCLK
I2C_SD
GPIO_0
UART_TXD1
UART_RXD1
UART_RXD0
UART_TXD0
I2S_CLK
I2S_WS
I2S_SDI
I2S_SDO
REF_CLK0
R9
5.1K
R7
R10
CPURST_N
WPS_RST_PBC
PORST_N
WDT_RST_N
WLED_N
NC_1
C24
MT7688AN
U1D
AVDD33_USB
AVDD12_PCIE
AVDD33_PCIE
PERST_N
PCIE_CKP0
PCIE_CKN0
PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0
USB_VRT
USB_DP
USB_DM
PCIE_IO_VSS
C40
C41
4.7uF
C42
C43
0.1uF
R22
UD_P
UD_N
SOC_1.2VD
U1E
AVDD33_TX_P0
AVDD33_COM
AVDD33_TX_P1234_1
AVDD33_TX_P1234_2
C47
C48
EPHY_VRT
R26
24.3K 1%
Close to MT7688
DBG_JTAG_MODE=0
P4_LED_AN_MODE=2B01
P3_LED_AN_MODE=2B01
P2_LED_AN_MODE=2B01
P1_LED_AN_MODE=2B01
P0_LED_AN_MODE=2B00
GPIO39
GPIO40
GPIO41
GPIO42
LINK0
EPHY_LED4_N_JTRST_N
EPHY_LED3_N_JTCLK
EPHY_LED2_N_JTMS
EPHY_LED1_N_JTDI
EPHY_LED0_N_JTDO
MDI_TN_P4
MDI_TP_P4
MDI_RN_P4
MDI_RP_P4
MDI_TN_P3
MDI_TP_P3
MDI_RN_P3
MDI_RP_P3
MDI_TN_P2
MDI_TP_P2
MDI_RN_P2
MDI_RP_P2
MDI_TN_P1
MDI_TP_P1
MDI_RN_P1
MDI_RP_P1
MDI_TN_P0
MDI_TP_P0
MDI_RN_P0
MDI_RP_P0
EPHY_APGIO_AIP_EN[4:1]=4b1111
SD_MODE=2B00
SD_WP:0:write enable 1:write protect
SD_CD:0:card insert 1:no cardText
UART2_MODE=2B00
PWM1_MODE=2B00
PWM0_MODE=2B00
SPIS_MODE=2B01
SD_D2
SD_D3
SD_CMD
SD_CLK
SD_CD
SD_WP
SD_D0
SD_D1
RXD2/PWM3
TXD2/PWM2
PWM_CH1
PWM_CH0
GPIO15
GPIO14
GPIO17
GPIO16
TXO_N
TXO_P
RXI_N
RXI_P
SPI_CS1
SPI_MISO
SPI_MOSI
SPI_CS0
GPIO14
GPIO15
GPIO16
GPIO17
PWM_CH0
PWM_CH1
TXD2/PWM2
RXD2/PWM3
GPIO_0
SD_WP
UART_RXD0
UART_TXD0
SD_CD
SD_D1
RXI_P
PCIE_CKP0
PCIE_CKN0
PCIE_TXP0
PCIE_TXN0
WLED_N
UART_TXD1
UART_RXD1
VDD_FLASH
3.3VD
GND



[MT7688AN-IOT] 1. 1.8V for DDR2 2. 2.5V for DDR1 configured by SW



Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)